

# SUPPLEMENT

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BTEC  
GUIDANCE FOR STUDENTS

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## BUSINESS AND TECHNICIAN EDUCATION COUNCIL

### National Certificate in Telecommunications

Sets of model questions and answers for Business and Technician Education Council (BTEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits for questions are shown, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

#### BTEC: ELECTRONICS III

The questions in this paper are based on the BTEC's standard unit U81/743. Students are advised to read the notes above

Students should allow one hour to complete all the questions in Section A, and  $\frac{1}{2}$  hour for each of the questions in Section B.

#### SECTION A

**Q1** The following DC measurements were taken for the four-terminal network shown in Fig. 1. Calculate  $h_o$  and  $h_R$  for the following static condition:

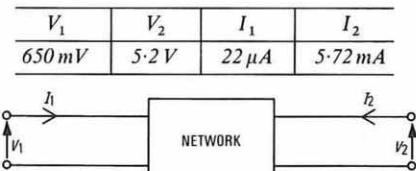


Fig. 1

A1

$$h_o = \frac{I_2}{V_2} = \frac{5.72 \times 10^{-3}}{5.2} \text{ S} = 1.1 \text{ mS.}$$

$$h_R = \frac{V_1}{V_2} = \frac{650 \times 10^{-3}}{5.2} = 0.125.$$

**Q2** Explain briefly, with the aid of a diagram, why the gain of the amplifier stage shown in Fig. 2 changes when the emitter bypass capacitor is disconnected.

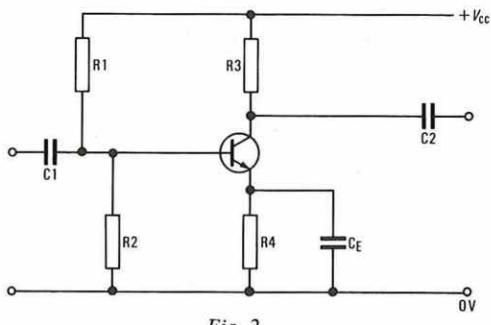
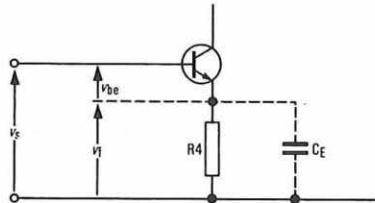


Fig. 2

**A2** The sketch shows a simplified amplifier input circuit when capacitor  $C_E$  is disconnected. The three voltages shown are alternating quantities (signal voltages).



[Tutorial note: The arrow used with each alternating voltage points to the end which is positive when the alternating quantity is positive.]

The effective input to the transistor is  $v_{be}$ ; thus the larger its value, the greater is the output voltage for a particular circuit.

From the sketch,

$$v_s = v_{be} + v_f.$$

$$\therefore v_{be} = v_s - v_f. \quad \dots \dots (1)$$

When capacitor  $C_E$  is connected, its low impedance at the signal frequency reduces the value of  $v_f$  to practically zero. Equation (1) now becomes:

$$v_{be} = v_s.$$

This condition results in a much larger output signal voltage. A considerably higher gain is thus obtained when capacitor  $C_E$  is connected.

**Q3** (a) Explain briefly what is meant by white noise.

(b) Give an example of this type of noise.

(c) State an example of a noise type which does not come into this category and describe how it differs.

**A3** (a) White noise has a flat frequency spectrum. The noise power per unit bandwidth is constant.

(b) An example of white noise is thermal noise.

[Tutorial note: RMS noise voltage =  $\sqrt{(4kRTB)}$ ,

where  $B$  is the bandwidth in hertz,

$T$  is the absolute temperature in kelvin,

$R$  is the resistance in ohms, and  
 $k$  is Boltzmann's constant.

But, noise power  $\propto$  (noise voltage)<sup>2</sup>.

$\therefore$  noise power  $\propto$  bandwidth.]

(c) An example of noise which is not white noise is *excess noise*. Excess noise does not have constant noise power per unit bandwidth. It is also called *flicker* and *1/f noise*. The latter name arises because the noise is inversely proportional to frequency. Excess noise has equal noise power per decade of frequency, and results from the fluctuations in the resistivity of the material from which the component is made. The noise voltage produced is proportional to the direct current flowing through the component.

**Q4** A communication system having unity gain has a signal-to-noise ratio of 46 dB. Determine the overall signal-to-noise ratio if two such systems are used in tandem.

**A4** Consider a noise-free test signal ( $S_1$ ) being fed into the first system. The signal power at the output of the first system =  $S_1$ .

Let the noise power at the output of the first system =  $N_1$ .

$$\therefore 46 = 10 \log_{10} \frac{S_1}{N_1} \quad \dots \dots (1)$$

The signal power at the output of the second system =  $S_1$ .

The noise power at the output of the second system =  $N_1 + N_2$ .

$$\text{The overall signal-to-noise ratio} = 10 \log_{10} \frac{S_1}{2N_1},$$

$$\begin{aligned} &= 10 \left( \log_{10} \frac{S_1}{N_1} - \log_{10} 2 \right), \\ &= 10 \log_{10} \frac{S_1}{N_1} - 10 \log_{10} 2. \quad \dots \dots (2) \end{aligned}$$

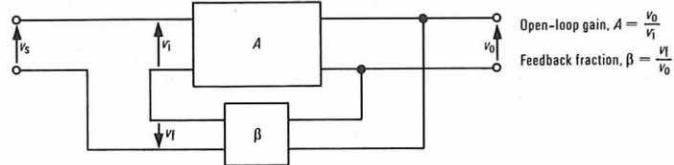
Substitute for  $10 \log_{10} \frac{S_1}{N_1}$  from equation (1) in equation (2).

$$\begin{aligned} \text{Overall signal-to-noise ratio} &= 46 - 10 \log_{10} 2, \\ &= 46 - 3 \text{ dB}, \\ &= \underline{43 \text{ dB}}. \end{aligned}$$

**Q5** Define positive feedback.

Explain briefly how an amplifier can become unstable as a result of positive feedback.

**A5** The sketch shows the block diagram of an amplifier with feedback.



$$\begin{aligned} \text{Closed-loop gain, } A_F &= \frac{v_o}{v_s}, \\ &= \frac{A}{1 - A\beta}. \quad \dots \dots (1) \end{aligned}$$

Feedback is 'positive' when the phase of the signal fed back ( $v_f$ ) is such as to increase the amplitude of the effective input signal ( $v_i$ ). Feedback is 'positive' when:

$$(1 - A\beta) < 1.$$

Therefore, the closed-loop gain ( $A_F$ ) is greater than the open-loop gain ( $A$ ).

An unstable condition exists when  $A\beta \rightarrow 1$ .

$$\therefore (1 - A\beta) \rightarrow 0.$$

$$\therefore A_F \rightarrow \infty.$$

Under this condition, no input is required to produce an output and an oscillatory state exists.

**Q6** In an amplifier using negative feedback, determine the feedback fraction required to reduce a previous open-loop voltage gain of 8000 to a closed-loop gain of 400.

**A6** Open-loop gain,  $A = 8000$ .

Closed-loop gain,  $A_F = 400$ ,

$$= \frac{A}{1 - A\beta},$$

where  $\beta$  is the feedback fraction.

$$\therefore 400 = \frac{8000}{1 - 8000\beta}.$$

$$400(1 - 8000\beta) = 8000.$$

$$400 - 32 \times 10^5 \beta = 8000.$$

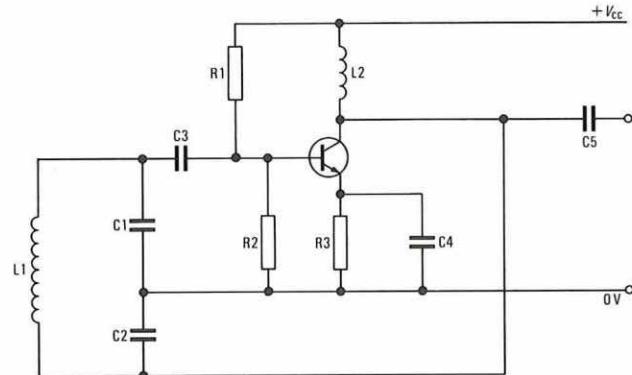
$$-32 \times 10^5 \beta = 7600.$$

$$\begin{aligned} \therefore \beta &= -\frac{7600}{32 \times 10^5}, \\ &= \underline{-2.375 \times 10^{-3}}. \end{aligned}$$

**Q7** Draw the circuit diagram of an LC oscillator.

Which components primarily determine the frequency of oscillations?

**A7** The circuit diagram of the oscillator is shown in the sketch.



The frequency-determining components are L1, C1 and C2.

*Tutorial note:*

$$\text{Frequency of oscillations, } f_0 \approx \frac{1}{2\pi\sqrt{(L_1 C_T)}} \text{ hertz,}$$

$$\text{where } C_T = \frac{C_1 \times C_2}{C_1 + C_2}.$$

The tuned circuit L1, C1 and C2 is at resonance when the total reactance around the circuit is zero. Let  $\omega_0 = 2\pi f_0$ . Thus,

$$X_{L1} = X_{C1} + X_{C2},$$

$$= \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2},$$

$$= \frac{1}{\omega_0} \left( \frac{1}{C_1} + \frac{1}{C_2} \right),$$

$$= \frac{1}{\omega_0} \left( \frac{1}{C_T} \right). \quad \left( \frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \right)$$

$$\therefore \omega_0 L_1 = \frac{1}{\omega_0 C_T}.$$

$$\therefore \omega_0^2 = \frac{1}{L_1 C_T}.$$

$$\therefore \omega_0 = \frac{1}{\sqrt{(L_1 C_T)}}.$$

$$\therefore f_0 = \frac{1}{2\pi\sqrt{(L_1 C_T)}}.$$

**Q8** State two factors which affect the frequency stability of an oscillator. Explain briefly how the effects of the factors quoted can be reduced.

**A8 (a) Temperature Variation** This can cause variations in the values of the inductors and capacitors and consequently alter the resonant frequency of the frequency-determining circuit. The effects of temperature can be minimised by siting the frequency-determining components well away from any heat source and by providing good ventilation to reduce temperature changes. In certain cases, the frequency-determining circuit can be enclosed within a thermostatically controlled oven.

**(b) Load Variation** The load on an oscillator reflects an impedance back into the frequency-determining circuit. Load variations can therefore produce a shift in the frequency of oscillations, particularly if the load is reactive. Isolation of the load from the oscillator can be achieved by means of a buffer amplifier. The high input impedance of the buffer amplifier provides a light constant load for the oscillator.

**Q9** The circuit shown in Fig. 3 is an example of excessive positive feedback. Identify this circuit and briefly explain its action.

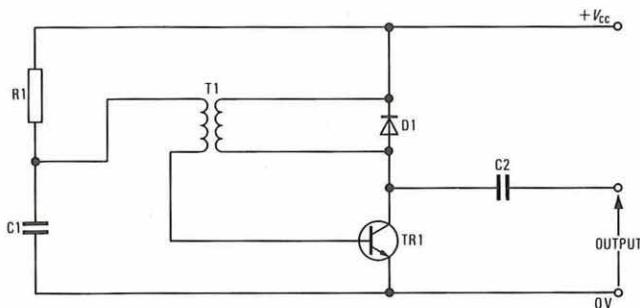


Fig. 3

**A9** The circuit shown in Fig. 3 is a blocking oscillator.

Positive feedback via transformer T1 ensures that, when the transistor initially conducts, it is driven rapidly into saturation. The reduced rate of increase of the collector current now causes a decrease in the feedback voltage to the base.

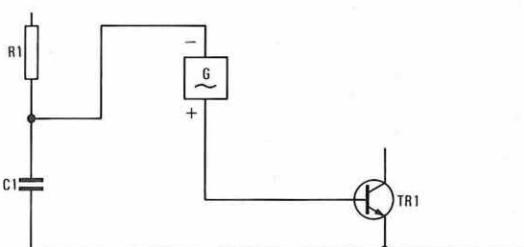
[Tutorial note: The reduced rate of change of the flux linking the secondary winding (base circuit) results in a smaller mutual induced EMF (feedback voltage) in the secondary.]

The reduction in the positive feedback voltage to the base causes a decrease in the collector current. This produces a change in the polarity of the feedback voltage, resulting in the transistor becoming cut off.

[Tutorial note: The reduction in the collector current causes a decrease in the flux linking the secondary of transformer T1 and thus produces a reversal of the polarity of the mutual induced EMF in the secondary.]

The transistor is held cut off by the charge acquired by capacitor C1 during the transistor's conducting interval.

[Tutorial note: The apparent contradiction of a positive on the base, and the top plate of capacitor C1 charging negative can be seen to be true by considering the sketch.



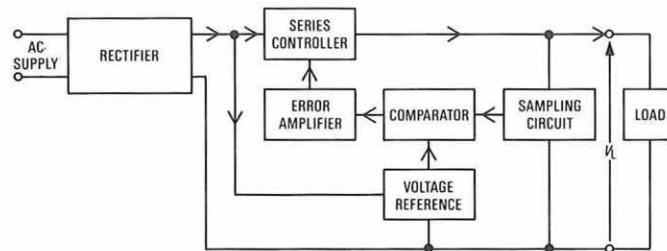
The secondary of transformer T1 has been replaced by an equivalent generator. The polarity of the generator output is for the circuit condition when the collector current is initially increasing.]

The transistor remains cut off until capacitor C1 discharges/charges sufficiently through resistor R1 to raise the base potential above cut off.

The action is then repeated.

**Q10** Sketch the block diagram of a series stabilised power supply that uses the comparator technique.

**A10**



## SECTION B

**Q11** The data for the two-stage transistor amplifier shown in Fig. 4 is as follows:

$$TR1 \quad h_{ie} = 6 \text{ k}\Omega$$

$$h_{fe} = 120$$

$$h_{oe} = 20 \mu\text{s}$$

$$TR2 \quad h_{ie} = 3.8 \text{ k}\Omega$$

$$h_{fe} = 150$$

$$h_{oe} = 25 \mu\text{s}$$

(a) Sketch the equivalent circuit of the two-stage amplifier at its mid-band frequencies.

Indicate the values of all the components shown in your sketch.

(b) Estimate the following using your equivalent circuit:

(i) The signal voltages  $v_2$  and  $v_3$  if the input signal voltage,  $v_1$ , is 0.8 mV. Assume the signal is at a mid-band frequency.

(ii) The lower 3 dB frequency.

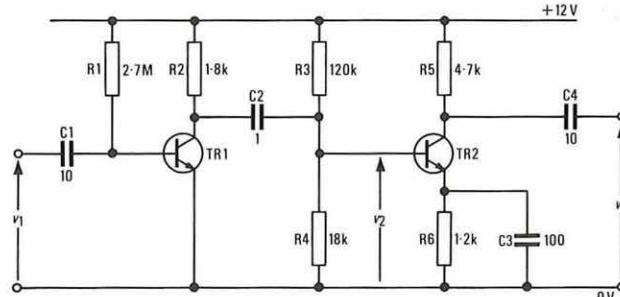
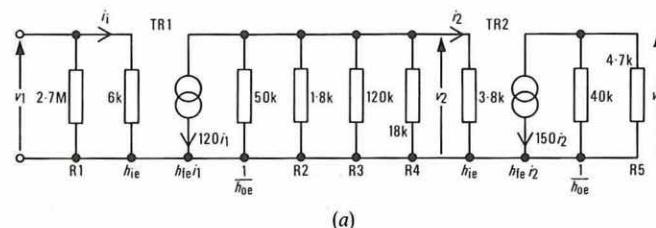


Fig. 4

**A11 (a)** [Tutorial note: The reactances of the capacitors C1, C2, C3 and C4 would be negligible at the mid-band frequencies. These capacitors, together with resistor R6, thus do not appear on the equivalent circuit.]

The equivalent circuit is shown in sketch (a).



$$(b) (i) \text{ Input current of transistor TR1, } i_1 = \frac{v_1}{h_{ie}},$$

$$= \frac{0.8 \times 10^{-3}}{6 \times 10^3} \text{ A,}$$

$$= 0.133 \times 10^{-6} \text{ A.}$$

Total load on transistor TR1 is given by:

$$\begin{aligned} \frac{1}{R_{L1}} &= \frac{1}{h_{oe}} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{h_{ie}}, \\ &= \frac{1}{50} + \frac{1}{1.8} + \frac{1}{120} + \frac{1}{18} + \frac{1}{3.8} \quad (\text{where } R_{L1} \text{ is in k}\Omega). \\ \therefore R_{L1} &= 1.108 \text{ k}\Omega. \end{aligned}$$

Signal voltage,  $v_2 = -h_{fe} i_1 R_{L1}$ ,

$$\begin{aligned} &= -120 \times 0.133 \times 10^{-6} \times 1.108 \times 10^3 \text{ V}, \\ &= \underline{-17.68 \text{ mV}}. \end{aligned}$$

Input current of transistor TR2,

$$\begin{aligned} i_2 &= \frac{v_2}{h_{ie}} = \frac{-17.68 \times 10^{-3}}{3.8 \times 10^3} \text{ A}, \\ &= -4.65 \times 10^{-6} \text{ A}. \end{aligned}$$

Total load on transistor TR2 is given by:

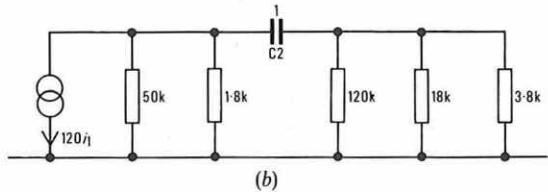
$$\begin{aligned} R_{L2} &= \frac{\frac{1}{h_{oe}} \times R_s}{\frac{1}{h_{oe}} + R_s} = \frac{40 \times 4.7}{40 + 4.7}, \\ &= 4.21 \text{ k}\Omega. \end{aligned}$$

Signal voltage,  $v_3 = -h_{fe} i_2 R_{L2}$ ,

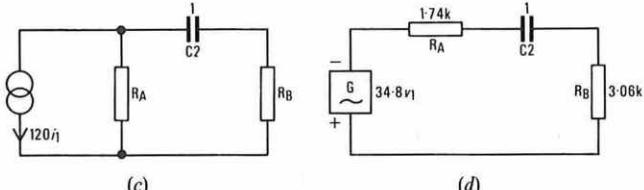
$$\begin{aligned} &= -150 \times (-4.65 \times 10^{-6}) \times 4.21 \times 10^3 \text{ V}, \\ &= \underline{2.94 \text{ V}}. \end{aligned}$$

(ii) [Tutorial note: The reduction in gain at low frequencies is due to the increased reactance of the coupling capacitors  $C_1$ ,  $C_2$  and  $C_4$ .]

In the two-stage amplifier circuit shown in Fig. 4 the capacitance of the coupling capacitor  $C_2$  is considerably smaller than the capacitances of  $C_1$  and  $C_4$ . The initial low-frequency gain reduction thus depends on capacitor  $C_2$  and the associated circuit shown in sketch (b). The initial simplification of this circuit is shown in sketch (c).



(b)



(c)

(d)

In sketch (c),

$$R_A = \frac{50 \times 1.8}{50 + 1.8} \text{ k}\Omega = 1.74 \text{ k}\Omega.$$

$$\frac{1}{R_B} = \frac{1}{120} + \frac{1}{18} + \frac{1}{3.8} \quad (\text{where } R_B \text{ is in k}\Omega).$$

$$\therefore R_B = 3.06 \text{ k}\Omega.$$

Further simplification using Thévenin's theorem produces sketch (d).

[Tutorial note: The value of the output of the constant voltage generator is not required for the solution of this problem.]

The following condition exists in sketch (d) at the lower 3 dB frequency:

$$X_{C2} = R_A + R_B = 1740 + 3060 = 4800 \Omega.$$

$$\therefore \frac{1}{2\pi f_1 C_2} = 4800.$$

$$\begin{aligned} \text{Lower 3 dB frequency, } f_1 &= \frac{1}{2\pi \times 4800 \times C_2}, \\ &= \frac{1}{2\pi \times 4800 \times 1 \times 10^{-6}}, \\ &= \underline{33.16 \text{ Hz}}. \end{aligned}$$

Q12 (a) State the two main requirements of a high-fidelity audio-frequency output stage.

(b) A complementary power amplifier and driver stage is shown in Fig. 5; describe the operation of this circuit.

(c) Explain, with the aid of a circuit diagram, how the circuit shown in Fig. 5 can be modified to reduce the unwanted effects of temperature variation.

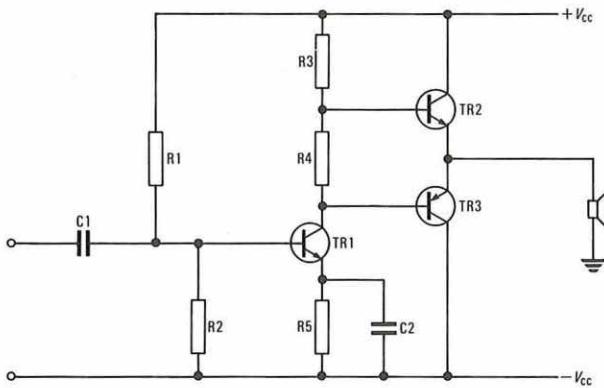


Fig. 5

A12 (a) The two main requirements are:

- to provide the required audio power output into a low-impedance loudspeaker load (typically, 4, 8 and 15  $\Omega$ ), and
- to ensure that any distortion present at the output is minimal.

(b) The operating condition of the driver stage, transistor TR1, is class A. This is achieved by means of the potential divider consisting of resistors R1 and R2, together with the emitter resistor R5. Capacitor C2 decouples the emitter of transistor TR1 to prevent negative feedback.

The collector load of transistor TR1 is resistor R3.

The output stage, comprising transistors TR2 and TR3, is operated in class AB; a small quiescent current flows through transistors TR2 and TR3 in the no-signal condition. This is accomplished by the quiescent current of transistor TR1, together with resistor R4, which produces an offset bias voltage for the bases of transistors TR2 and TR3.

The low output impedance of the emitter-follower configuration of transistors TR2 and TR3 enables a low-impedance loudspeaker load to be fed direct. The input signal is coupled by capacitor C1 to the base of transistor TR1, and this causes the collector current to vary about its quiescent value. The output of transistor TR1, which is the fluctuating voltage across resistor R3, is applied to the bases of the output transistors TR2 and TR3.

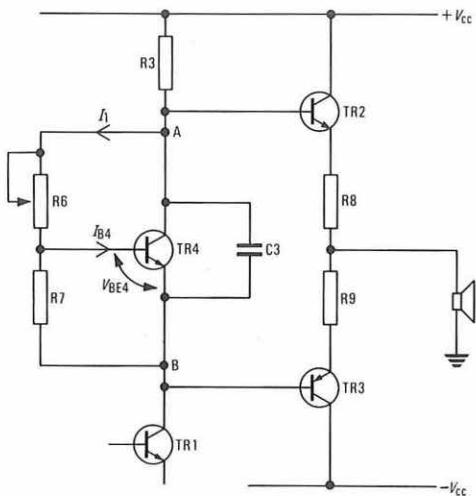
On the positive-going half cycle of the signal, the conduction of transistor TR2 is increased and transistor TR3 is cut off. The signal current flows from  $+V_{cc}$ , through transistor TR2 and down through the loudspeaker load to earth. On the negative-going half cycle of the signal, transistor TR3 increases conduction and transistor TR2 is cut off. The signal current now flows from earth up through the loudspeaker and transistor TR3 to  $-V_{cc}$ , so completing the signal cycle at the output.

(c) The modifications to the circuit are shown in the sketch.

Temperature changes affect the parameters of the output transistors and, as a consequence, the optimum value of the offset bias voltage varies with temperature. This effect can be counteracted by replacing resistor R4 with transistor TR4, and resistors R6 and R7.

Transistor TR4 conducts throughout the cycle of the input signal, and its operating condition stabilises with  $V_{BE4}$  at about 0.6 V. The value of resistor R7 is chosen so that the current  $I_1$  is much greater than the base current  $I_{B4}$ ; consequently, the potential difference between points A and B is given by

$$\begin{aligned} V_{AB} &= I_1(R_6 + R_7), \\ &= \frac{V_{BE4}}{R_7} (R_6 + R_7), \\ &= V_{BE4} \left( \frac{R_6}{R_7} + 1 \right). \end{aligned}$$



Resistor R6 is adjusted to provide the optimum value of the offset bias voltage. The offset voltage,  $V_{AB}$ , which depends on transistor TR4, is now affected by temperature in the same manner as the base-emitter voltages of transistors TR2 and TR3. Temperature compensation can thus be achieved by mounting transistor TR4 on the heat sink of transistors TR2 and TR3, to ensure that all three transistors are operating at the same temperature.

[Tutorial note: The circuit, consisting of transistor TR4, and resistors R6 and R7, is sometimes called the *amplified diode*. This name arises from the fact that  $V_{AB}$  is a multiple of the voltage drop across the forward-biased base-emitter junction of transistor TR4.]

Capacitor C3 acts as a signal bypass of transistor TR4, ensuring that both the bases of the output transistors have the same signal voltage applied. The addition of the resistors R8 and R9 improves the stability of the quiescent condition of transistors TR2 and TR3 against temperature change. Any tendency for the quiescent collector current to rise as a result of temperature increase produces a larger voltage across resistors R8 and R9; this effectively reduces the base-emitter voltages of the output transistors and counteracts the rise in the quiescent collector current.

[Tutorial note: Resistors R8 and R9 are low-value resistors (typically  $0.5\ \Omega$ ) in order to keep any power loss in these resistors to a minimum.]

**Q13** (a) Explain, with the aid of diagrams, how negative feedback affects the following properties of an amplifier:

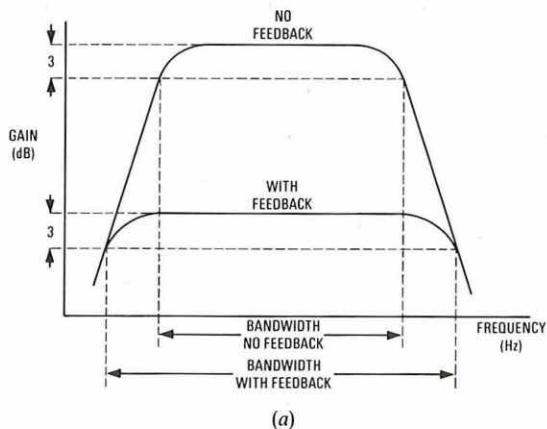
- (i) bandwidth, and
- (ii) input impedance.

(b) Show, with the aid of a circuit diagram, how series voltage negative feedback can be used with an operational amplifier.

Derive an expression for the feedback fraction of this amplifier circuit.

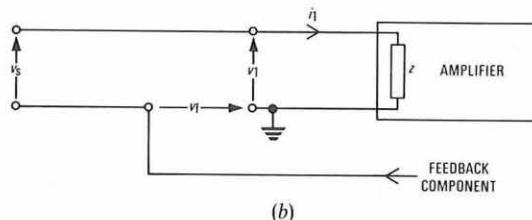
**A13** (a) (i) In an amplifier, a variation in gain can occur because of the impedances of reactive components changing with frequency.

The use of negative feedback causes a reduction in gain, but also a decrease in the gain variation. The overall effect is to increase the bandwidth of the amplifier (see sketch (a)).



[Tutorial note: The gain-bandwidth product remains almost constant.]

(ii) The input impedance of an amplifier depends on how the feedback is applied in the input circuit; that is, whether the feedback component is applied in series or in parallel with the input signal. Sketch (b) shows an example of series negative feedback.



In a series negative feedback circuit, the feedback component is a voltage ( $v_f$ ).

The feedback voltage ( $v_f$ ) is combined in series with the input voltage ( $v_s$ ).

$$\text{Effective input, } v_i = v_s - v_f \quad (v_f \text{ is in antiphase to } v_s). \quad \therefore v_s = v_i + v_f \quad \dots \dots (1)$$

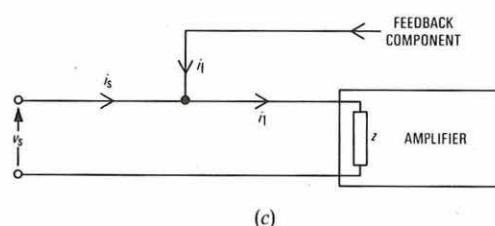
With no feedback ( $v_f = 0$ )

$$\begin{aligned} \text{Input Impedance, } z_{in} &= \frac{v_s}{i_1}, \\ &= \frac{v_i}{i_1} \quad (v_i = v_s \text{ when } v_f = 0), \\ &= z. \end{aligned}$$

With feedback:

$$\begin{aligned} \text{Input Impedance, } z_{in} &= \frac{v_s}{i_1}, \\ \text{As } v_s > v_i & \quad (\text{refer to equation (1)}), \\ \frac{v_s}{i_1} &> \frac{v_i}{i_1}, \\ \therefore z_{in} &> z. \end{aligned}$$

Therefore, series negative feedback increases the input impedance. Sketch (c) shows an example of parallel negative feedback.



In a parallel negative feedback circuit, the feedback component is a current ( $i_f$ ).

The feedback current ( $i_f$ ) is combined in parallel with the input current ( $i_s$ ).

$$\begin{aligned} \text{Effective input, } i_1 &= i_s - i_f \quad (i_f \text{ is in anti-phase to } i_s). \\ \therefore i_s &= i_1 + i_f. \quad \dots \dots (2) \end{aligned}$$

With no feedback ( $i_f = 0$ ):

$$\begin{aligned} \text{Input impedance, } z_{in} &= \frac{v_s}{i_s}, \\ &= \frac{v_s}{i_1} \quad (i_1 = i_s \text{ when } i_f = 0), \\ &= z. \end{aligned}$$

With feedback:

$$\text{Input impedance, } z_{in} = \frac{v_s}{i_s}.$$

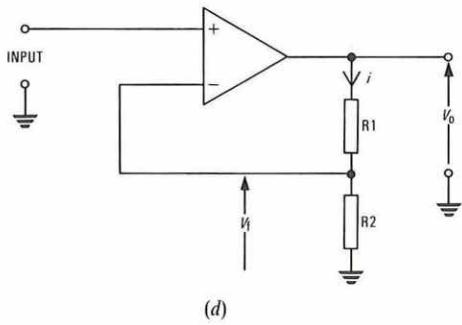
As  $i_s > i_1$  (refer to equation (2)).

$$\frac{v_s}{i_s} < \frac{v_s}{i_1}.$$

$$\therefore z_{in} < z.$$

Therefore, parallel negative feedback reduces the input impedance.

(b) Sketch (d) shows an operational amplifier with series voltage negative feedback.



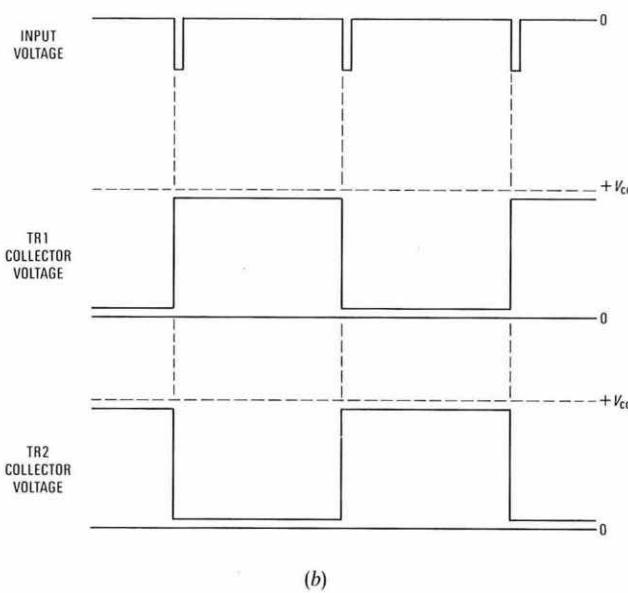
(d)

The current flowing into the operational amplifier is negligible because of the very high input impedance. The same current,  $i$ , therefore flows through both resistors R1 and R2 in sketch (d).

$$\text{Feedback voltage, } v_f = iR_2.$$

$$\text{Output voltage, } v_o = i(R_1 + R_2).$$

$$\begin{aligned} \text{Feedback fraction, } \beta &= \frac{v_f}{v_o}, \\ &= \frac{iR_2}{i(R_1 + R_2)}, \\ &= \frac{R_2}{R_1 + R_2}. \end{aligned}$$



(b)

TR1 is sufficiently positive for the transistor to be conducting heavily. The collector of transistor TR1 is consequently almost at zero potential, causing the base of transistor TR2 to be negative and thus hold transistor TR2 off.

The diodes, D1 and D2, are called *steering diodes*, as they direct the negative input pulse to the base of the conducting transistor. In the initial circuit condition shown by the waveforms, the base of transistor TR2 is negative, causing diode D2 to be reverse biased. Diode D1, at this instant, is forward biased because the base of transistor TR1 is slightly positive.

On the arrival of a negative trigger pulse at the junction of the two diodes, the conduction of diode D1 increases. This results in a fall in the base potential of transistor TR1, and it is cut off. The potential at the collector of transistor TR1 now rises to almost  $+V_{cc}$ . The rise at the collector of transistor TR1 causes the base of transistor TR2 to become sufficiently positive for it to conduct heavily and its collector potential falls to almost zero. This fall reinforces the initial fall at the base of transistor TR1, so maintaining transistor TR1 in a cut off condition.

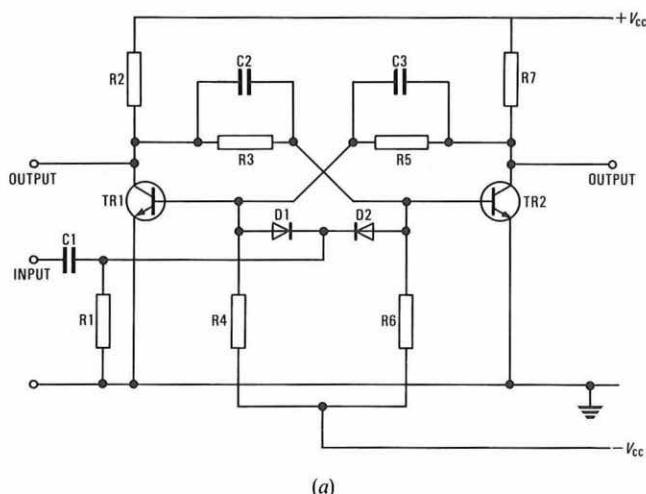
The circuit remains in this state until the arrival of the next negative trigger pulse. The state of the two diodes has also changed. Diode D1 is now reverse biased by the negative potential on the base of transistor TR1, while diode D2 is forward biased. The next negative trigger pulse is thus directed to the base of transistor TR2, so reversing the states of the two transistors. Capacitors C2 and C3 are called *speed-up capacitors*. They ensure that a larger change in potential is initially coupled from each collector to the opposite base and a more rapid switching action during a change in state.

[Tutorial note: No significant rounding of the positive-going leading edge occurs, provided the speed-up capacitors have a small value; for example, a value of 100 pF is suitable at a switching frequency of 1 kHz.]

The input to a bistable circuit is frequently a square wave. In this event, the time constant of capacitor C1 and resistor R1 is arranged to be short compared with the period of the square wave, and a form of differentiation occurs. The waveform at the junction of the diodes now consists of positive- and negative-going pulses, as shown in sketch (c). Only the negative pulses trigger the bistable circuit, so producing an output of half the frequency of the input waveform at each collector.

**Q14** Explain, with the aid of a circuit and waveform diagrams, the operation of a bistable multivibrator.

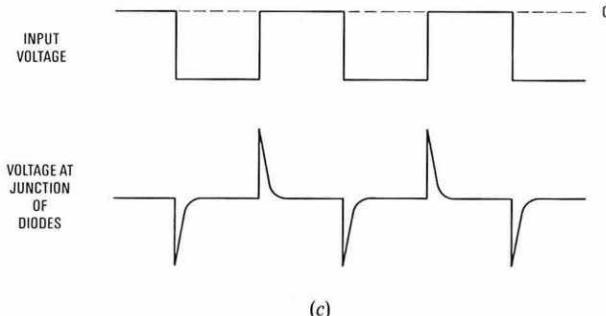
**A14** The circuit diagram of a bistable multivibrator is shown in sketch (a).



(a)

A bistable multivibrator has two stable states. A change of state occurs only when a pulse of the required polarity appears at the input. The two stable states are the result of the DC coupling between the two transistors.

The waveforms for the circuit, shown in sketch (b), start with transistor TR2 initially cut off. The collector of transistor TR2 is at a positive potential close to  $+V_{cc}$ . This ensures that the base of transistor



(c)

Questions and answers contributed by C. Wright

The following questions are based on the BTEC's standard unit U80/691. Students are advised to read the notes on p. 17

**Q1** The frequency for a parallel circuit is given by the formula

$$f = \frac{1}{2\pi} \sqrt{\left(\frac{1}{LC} - \frac{R^2}{L^2}\right)}.$$

Transpose the formula to make  $R$  the subject.

(20 min)

$$\mathbf{A1} \quad f = \frac{1}{2\pi} \sqrt{\left(\frac{1}{LC} - \frac{R^2}{L^2}\right)}.$$

Multiplying both sides of the formula by  $2\pi$  gives

$$2\pi f = \sqrt{\left(\frac{1}{LC} - \frac{R^2}{L^2}\right)}.$$

Squaring both sides gives

$$4\pi^2 f^2 = \frac{1}{LC} - \frac{R^2}{L^2}.$$

Adding  $\frac{R^2}{L^2}$  to both sides gives

$$4\pi^2 f^2 + \frac{R^2}{L^2} = \frac{1}{LC}.$$

Multiplying both sides by  $L^2$  gives

$$4\pi^2 f^2 L^2 + R^2 = L^2 \times \frac{1}{LC}.$$

Cancelling  $L$  on the right-hand side of the formula gives

$$4\pi^2 f^2 L^2 + R^2 = \frac{L}{C}.$$

Subtracting  $4\pi^2 f^2 L^2$  from both sides of the formula gives

$$R^2 = \frac{L}{C} - 4\pi^2 f^2 L^2.$$

Taking the square root of both sides gives

$$R = \sqrt{\left(\frac{L}{C} - 4\pi^2 f^2 L^2\right)} = \sqrt{\left(\frac{L - 4\pi^2 f^2 L^2 C}{C}\right)}.$$

**Q2** Given the formula

$$L = \frac{gt^2}{4\pi},$$

draw up a table of values for  $L$ , to 2 significant figures, for values of  $t$  from 1 s to 3 s at intervals of 0.5 s, given  $\pi = 3.142$  and  $g = 9.81 \text{ m/s}^2$ . Also state the units of  $L$ . (15 min)

**A2**

$t$	1	1.5	2	2.5	3
$t^2$	1	2.25	4	6.25	9
$gt^2$	9.81	22.1	39.2	61.3	88.3
$4\pi$	12.6	12.6	12.6	12.6	12.6
$L$	0.78	1.7	3.1	4.9	7.0

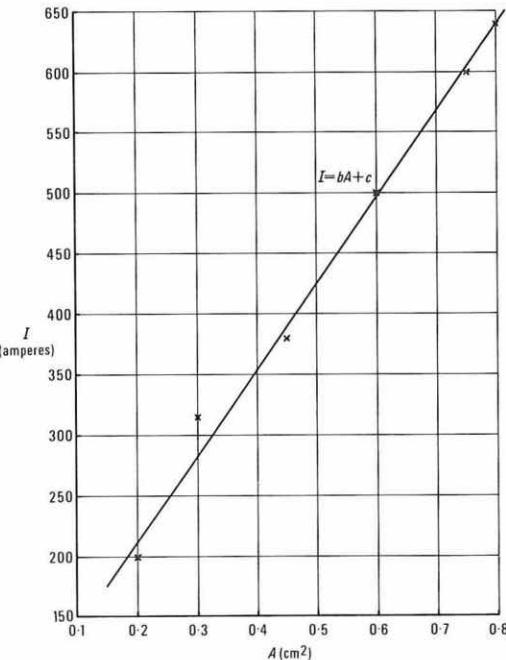
The units of  $L$  are metres/second<sup>2</sup> × second<sup>2</sup> = metres.

**Q3** The maximum safe current  $I$  amperes for a cable of  $A$  square centimetre cross-section is given in the following table of values.

$I$	200	315	380	500	600	640
$A$	0.2	0.3	0.45	0.6	0.75	0.8

The law connecting  $I$  and  $A$  is thought to be of the form  $I = bA + c$  show that this is true and obtain suitable values for  $b$  and  $c$ . (40 min)

**A3** The sketch shows the points plotted on a graph. A straight line can be drawn that passes very close to all the points; thus, the graph follows the law  $I = bA + c$ .



From the graph, when  $I = 570$ ,  $A = 0.7$ , and when  $I = 280$ ,  $A = 0.3$ .

Substituting these values in the equation gives

$$570 = 0.7b + c, \text{ and} \quad (1)$$

$$280 = 0.3b + c. \quad (2)$$

Subtracting equation (2) from equation (1) gives

$$290 = 0.4b.$$

$$\therefore b = \frac{290}{0.4} = 725.$$

Substituting  $b = 725$  in equation (1) gives

$$570 = 0.7 \times 725 + c.$$

$$\therefore 570 = 507.5 + c.$$

$$\therefore c = 570 - 507.5. \\ = 62.5.$$

Therefore, the equation of the straight line is

$$I = 725A + 62.5.$$

**Q4** It is known that a straight line passes through the points  $(1, -3)$  and  $(4, 2)$ . Without drawing the graph, find the equation of the straight line given that the general equation of a straight line is  $y = mx + c$ . (15 min)

**A4** The given point  $(1, -3)$  means that when  $x = 1$ ,  $y = -3$ , and the given point  $(4, 2)$  means that when  $x = 4$ ,  $y = 2$ .

Substituting for both sets of values in the equation  $y = mx + c$  gives

$$-3 = m + c, \text{ and} \quad (1)$$

$$2 = 4m + c \quad (2)$$

Subtracting equation (2) from equation (1) gives

$$-5 = -3m.$$

$$\therefore m = \frac{5}{3}$$

Substituting  $m = \frac{5}{3}$  in equation 1 gives

$$-3 = \frac{5}{3} + c.$$



$$\begin{aligned}\text{Area of sector OCD} &= \frac{1}{2} \times 20^2 \times 0.6 \\ &= 200 \times 0.6 \\ &= 120 \text{ mm}^2.\end{aligned}$$

$$\therefore \text{Area of shaded cross-section} = 480 - 120, \\ = 360 \text{ mm}^2.$$

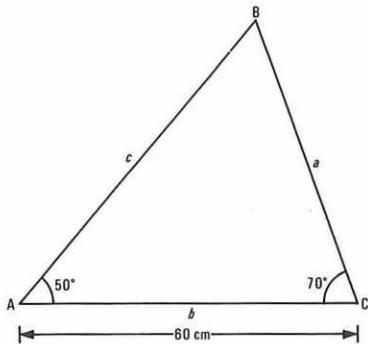
(b) The formula for the length of an arc of a sector is  $r\theta$ , where  $\theta$  is measured in radians.

$$\therefore \text{Length of arc AB} = 40 \times 0.6, \\ = 24 \text{ mm.}$$

**Q8** A triangle ABC has angle A of  $50^\circ$ , angle C of  $70^\circ$  and side b of 60 cm. By using the sine rule, calculate the lengths of sides a and c. (20 min)

**A8** [Tutorial note: When labelling a triangle, small letters are used to represent the lengths of the sides opposite the angles.]

The given triangle is shown in the sketch.



The sine rule states that

$$\frac{a}{\sin A} = \frac{b}{\sin B} = \frac{c}{\sin C}.$$

To find side c, use  $\frac{b}{\sin B} = \frac{c}{\sin C}$ .

$$\therefore c = \frac{b \sin C}{\sin B}.$$

But,

$$B = 180^\circ - (A + C).$$

$$\begin{aligned}\therefore B &= 180^\circ - (50^\circ + 70^\circ), \\ &= 180^\circ - 120^\circ, \\ &= 60^\circ.\end{aligned}$$

$$\begin{aligned}\therefore c &= \frac{60 \times \sin 70^\circ}{\sin 60^\circ}, \\ &= \frac{60 \times 0.9400}{0.8660}, \\ &= 65.13 \text{ cm.}\end{aligned}$$

To find a, use  $\frac{a}{\sin A} = \frac{b}{\sin B}$ .

$$\begin{aligned}\therefore a &= \frac{b \sin A}{\sin B}, \\ &= \frac{60 \times \sin 50^\circ}{\sin 60^\circ}, \\ &= \frac{60 \times 0.766}{0.866}, \\ &= 53.1 \text{ cm.}\end{aligned}$$

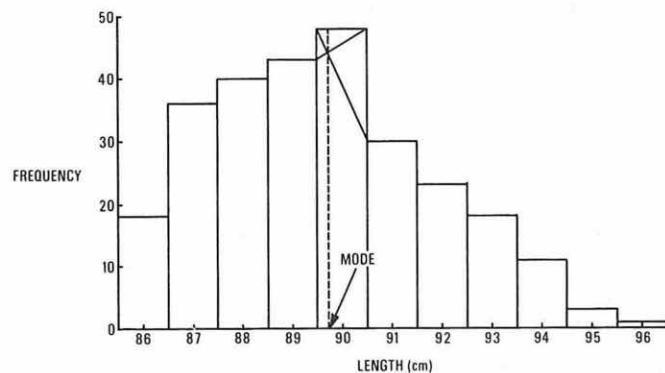
**Q9** The length of a group of wooden posts were measured to the nearest centimetre and the following results were obtained:

Length (cm)	86	87	88	89	90	91	92	93	94	95	96
Frequency	18	36	40	43	48	30	23	18	11	3	1

Find the mode of the distribution.

(15 min)

**A9** The sketch shows a histogram of the given data.



From the histogram, the mode = 89.7.

**Q10** Extensions to an existing telephone exchange are to be carried out in brickwork to match the original as near as possible. Sample measurements were taken of the combined length of three bricks and three joints (in millimetres) as follows:

685	715	695	685	725	705	675	695	705	715
725	695	665	705	695	655	665	675	685	655

(a) Construct a frequency distribution table for these results.

(b) Calculate their mean and standard deviation. (30 min)

**A10 (a)**

Length, x	Frequency, f	d	fd	$d^2$	$fd^2$
655	2	-40	-80	1600	3200
665	2	-30	-60	900	1800
675	2	-20	-40	400	800
685	3	-10	-30	100	300
695	4	0	0	0	0
705	3	10	30	100	300
715	2	20	40	400	800
725	2	30	60	900	1800
	$\Sigma f = 20$		$\Sigma fd = -80$		$\Sigma fd^2 = 9000$

(b) Let assumed mean  $\bar{A} = 695$ .

$$\text{Mean } \bar{x} = \bar{A} + \frac{\Sigma fd}{\Sigma f},$$

$$= 695 + \frac{-80}{20},$$

$$= 695 - 4,$$

$$= 691 \text{ cm.}$$

$$\text{Standard deviation} = \sqrt{\left(\frac{\Sigma fd^2}{\Sigma f} - \left(\frac{\Sigma fd}{\Sigma f}\right)^2\right)},$$

$$= \sqrt{\left(\frac{9000}{20} - (4)^2\right)},$$

$$= \sqrt{450 - 16},$$

$$= \sqrt{434},$$

$$= 20.83.$$

*[Tutorial note: Some of the questions given below require a knowledge of the mnemonics and machine code of a specific microprocessor. It would clearly be impossible to duplicate all such questions and answers for a range of microprocessors. Therefore, the Zilog Z80 has been chosen as a representative microprocessor because of its widespread use and machine-code compatibility with the Intel 8080 and 8085. Students who have studied the Rockwell 6502 or Motorola 6800 should not find too much difficulty in adapting the questions for those microprocessors.]*

A shortened instruction set for the Z80 is given below.

Mnemonic	Hexadecimal Code	Comment
LD A, n	3E n	Load the accumulator (register A) with data n.
LD A, B	78	Load the accumulator with the contents of register B.
LD B, n	06 n	Load register B with data n.
LD (HL), B	70	Load address (HL) from the accumulator.
LD L, n	2E n	Load register L with number n.
LD C, B	48	Load register C from B
LD HL, nn	21 nn	Load register pair HL with the number nn.
LD A, (HL)	7E	Load the accumulator from address (HL)
LD (HL), A	77	Load address (HL) from the accumulator.
ADD A, (HL)	86	Add the contents of address (HL) to the accumulator.
ADD A, B	80	Add the contents of register B to the accumulator.
AND B	A0	Logical AND the contents of register B with the contents of the accumulator.
SUB n	D6 n	Subtract number n from the accumulator.
INC HL	23	Increment register pair HL by 1.
INC A	3C	Increment the accumulator by 1.
INC C	0C	Increment register C
DEC HL	2B	Decrement register pair HL by 1.
DEC A	3D	Decrement the accumulator by 1.
CALL nn	CD nn	Call subroutine at address nn
JP nn	C3 nn	Jump to address nn.
JP Z nn	CA nn	Jump on zero to address nn.
JP NZ nn	C2 nn	Jump on non-zero to address nn.
HALT	76	Halt.

**Q1** Briefly explain why the binary number system is generally used to describe the operation of computers. (2 min)

**A1** The logic circuits used in computers are made up of transistors, which operate in one of two states, either ON or OFF. Therefore, it is convenient to represent these states as a HIGH logic level or a LOW logic level. Binary numbers also have two possible values, known as 1 or 0. Therefore, the two states in computer circuits can be represented by the two possible binary values, making it convenient to use binary arithmetic to explain the action of computer circuits.

**Q2** Briefly explain why the hexadecimal numbering system is used in preference to binary in connection with microcomputer programming. (2 min)

**A2** Although all computers work in binary, it is very difficult for programmers or operators to remember long strings of binary digits. Since hexadecimal numbers are produced by combining groups of four binary digits (four bits), it is far more convenient to use hexadecimal numbers in computer programming. The numbers generated have fewer digits and are therefore easier to remember. The use of hexadecimal numbers also makes the task of entry into the computer very much easier from simple keypads.

Since each hexadecimal character represents four binary digits, the task of representing the eight bits of the data bus and the sixteen bits of the address bus in a typical microcomputer system is very simple; they can be represented by two and four hexadecimal characters, respectively.

**Q3** Construct a table showing the decimal, binary, octal and hexadecimal numbers from 0 to 20. (4 min)

A3

Decimal	Binary	Octal	Hexadecimal
0	00000	0	0
1	00001	1	1
2	00010	2	2
3	00011	3	3
4	00100	4	4
5	00101	5	5
6	00110	6	6
7	00111	7	7
8	01000	10	8
9	01001	11	9
10	01010	12	A
11	01011	13	B
12	01100	14	C
13	01101	15	D
14	01110	16	E
15	01111	17	F
16	10000	20	10
17	10001	21	11
18	10010	22	12
19	10011	23	13
20	10100	24	14

**Q4** Perform the following calculations using a two's complement method, and check your answers in decimal.

(a) 100100–10101  
(b) 11001–11100

(8 min)

**A4** (a) Find the two's complement of 10101.

$$\begin{array}{r} 010101 \\ \text{Invert} \quad 101010 \\ \text{Add 1} \quad \underline{1} \\ 101011 \end{array} \quad [\text{Add a leading 0}]$$

Subtract by adding the two's complement.

$$\begin{array}{r} 100100 \\ 101011 \\ \underline{1} \\ 001111 \\ \uparrow \\ \text{overflow} \\ (\text{ignore}) \end{array}$$

Thus 100100–10101 = 1111.

In decimal, 100100 = 36,  
10101 = 21, and  
1111 = 15.

Thus 36 – 21 = 15, which is correct.

(b) Find the two's complement of 11100.

$$\begin{array}{r} 11100 \\ \text{Invert} \quad 00011 \\ \text{Add 1} \quad \underline{1} \\ 00100 \end{array}$$

Subtract by adding the two's complement.

$$\begin{array}{r} 11001 \\ 00100 \\ \underline{11101} \end{array}$$

No overflow indicates that the number is negative. Its value is found by calculating the two's complement of the answer.

$$\begin{array}{r} 11101 \\ \text{Invert} \quad 00010 \\ \text{Add 1} \quad \underline{1} \\ 00011 \end{array}$$

Thus 11001 – 11100 = –00011.

In decimal, 11001 = 25,  
11100 = 28, and  
11101 in two's-complement form represents –3.  
Thus 25 – 28 = –3, which is correct.

**Q5** (a) With reference to a microcomputer system, explain what is meant by the term 'bus'. (8 min)

(b) Briefly explain the function of the main buses.

**A5** (a) A bus is a group of conductors that are functionally related. In a computer system there are three major buses, the address bus, the data bus and the control bus.

(b) **Address Bus**

The address bus is a group of conductors that indicates which part of a microprocessor system is to operate at any moment. Generally, the address bus contains 16 separate wires and, therefore, is capable of accessing  $2^{16}$  (65 536) different memory locations within the system. The address bus is unidirectional; that is, addresses originate in the central processing unit (CPU) and are sent to all other devices in the system.

**Data Bus**

The data bus is a group of conductors that carries both the commands and the data between all the devices in a microprocessor system. Generally, an eight-bit microprocessor has eight data lines. In comparison with the address bus, these data lines are bidirectional; that is, data can be transferred both in and out of the CPU, memory devices, and input/output ports.

**Control Bus**

The control bus is a group of conductors that carries signals that synchronise the whole of the operation of the microprocessor system. Typically, this may include reading to and writing from memory, reading to and writing from input/output devices, interrupts, reset, wait etc. Some signals on the control bus originate within the microprocessor; others are originated by the peripheral devices. Different CPUs have different requirements for control signals and there is, therefore, no standard number of lines in the control bus.

**Q6** Briefly explain what is meant by the *FETCH/EXECUTE* cycle in a microprocessor. (4 min)

**A6** The *FETCH/EXECUTE* cycle refers to a sequence of events that every computer must carry out in order to operate any program. Each program instruction is individually fetched and executed in turn. The *FETCH* part of the cycle refers to the operation by which the computer obtains the next instruction from memory. To do this, the computer first places an address on the address bus, and sends a control signal to implement a memory read operation. A short time later, it reads in the data supplied by the memory on the data bus into its instruction register.

The *EXECUTE* part of the cycle refers to the time when the computer actually carries out the instruction. This may consist of a simple internal CPU operation which requires no further data from the memory. Alternatively, an additional memory read may be required in order to get more data upon which to operate. Once this data is obtained, it may be necessary for further machine cycles to be executed in order to complete the execution phase for the instruction.

**Q7** Use one of the answers below to complete the following sentence:  
'An algorithm is ...'

- (a) a set of instructions in the form of a computer program.
- (b) a set of mathematical tables.
- (c) a set of steps designed to show how a problem can be solved.
- (d) a pictorial representation of a computer program.

(1 min)

**A7** (c) a set of steps designed to show how a problem can be solved.

**Q8** Briefly describe the function of a monitor program within a micro-computer system. (4 min)

**A8** A monitor program in a small microcomputer system is one which generally executes as soon as the computer is switched on. For this reason, the monitor program, is normally resident in a read-only memory (ROM). Its main functions are to allow the user easy access to the computer memory, since the programs in the monitor include such features as keyboard scanning, output to a display, tape reading and writing etc. In addition, some simple facilities generally exist which allow the user to enter numbers in hexadecimal form directly into the computer memory, to tabulate these in a convenient manner, and to execute the programs which are written in this way. More sophisticated monitor programs may include facilities such as tracing the execution of a program by allowing direct access to information in a register at each instruction step. This may also include a single-step facility.

**Q9** What is meant by the term 'addressing mode'? Explain your answer with examples of two different addressing modes found in a common micro-processor instruction set. (5 min)

**A9** An addressing mode is the means used by a computer to determine the location of the data to be operated upon by an instruction.

Two common addressing modes are register and direct addressing; these are illustrated in the examples below.

**Register Addressing**

The instruction LD A, B is an example of register addressing, since the location of the data is determined by the names of the registers used in the instruction.

**Direct Addressing**

The instruction LD (1800H), A is an example of an instruction that uses direct addressing. In this particular case, the address which receives the data is specified as part of the instruction.

[Tutorial note: The answer to this question could have included many other types of addressing mode, including indirect addressing, implied addressing, indexed addressing, relative addressing etc.]

**Q10** The trace table given below was obtained from a computer program that contains only load instructions. By examining the table, write down the program which produced it.

PC	Registers								Memory	
	A	F	B	C	D	E	H	L	1850H*	1851H*
0100	00	00	00	00	00	00	00	00	00	00
0102	AA	00	00	00	00	00	00	00	00	00
0105	AA	00	00	00	00	00	18	50	00	00
0107	AA	00	BB	00	00	00	18	50	00	00
0108	AA	00	BB	00	00	00	18	50	BB	00
010A	AA	00	BB	00	00	00	18	51	BB	00
010B	AA	00	BB	BB	00	00	18	51	BB	00
010C	AA	00	BB	BB	00	00	18	51	BB	AA

\* Hexadecimal.

(5 min)

**A10** The program must be as follows:

Address	Mnemonic
0100	LD A, AAH
0102	LD HL, 1850H
0105	LD B, BBH
0107	LD (HL), B
0108	LD L, 51H
010A	LD C, B
010B	LD (HL), A

**Q11** For each of the instructions given below, state which of the general instruction groups they come from: the data transfer group, the arithmetic and logic group, or the flow of control group.

- (a) AND B
- (b) JP NZ, 1536H
- (c) HALT
- (d) LD HL, 6022H
- (e) CALL 0528H
- (f) ADD A, (HL)
- (g) INC C

(6 min)

**A11** (a) Arithmetic and logic group

- (b) Flow of control group
- (c) Flow of control group
- (d) Data transfer group
- (e) Flow of control group
- (f) Arithmetic and logic group
- (g) Arithmetic and logic group

**Q12** In a computer program, what is meant by the following terms:

- (a) loop, and
- (b) loop counter.

(5 min)

**A12** (a) A loop is the body of a program that may be repeated a number of times. Since the computer is an ideal tool for performing repetitive operations, loops form a very important part of many types of program.

(b) A loop counter is used to determine how many times a loop is repeated. Generally, the loop counter consists of a register that initially contains the number of loops to be executed. On each pass of the loop,

this number is decremented, and when it reaches 0 the loop is terminated. For microprocessors which contain only a limited number of registers, the loop counter can be set up easily in a memory address.

**Q13** With reference to Fig. 1, answer the following questions.

- What type of memory chip is shown?
- How many bits can be stored by the chip?
- How many eight-bit bytes can be stored by eight of these chips within a system? (4 min)

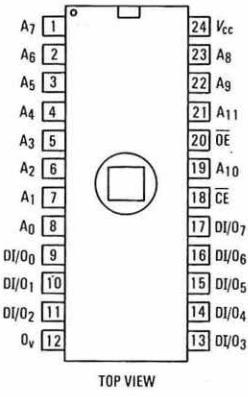


Fig. 1

**A13** (a) The device shown is an erasable programmable read-only memory

- One of the chips shown can store 32 768 bits.
- Eight such chips could store 32 Kbyte, each byte consisting of eight bits.

**Q14** Briefly explain the main differences between the two types of memory device commonly found in microprocessor systems. (4 min)

**A14** The two main types of memory found in microprocessor systems are random-access memory (RAM) and read-only memory (ROM); their main characteristics are indicated below.

#### RAM

RAM circuits hold data only while power is applied; that is, they are volatile. However, data can be written into them and read from them with a very fast access time.

#### ROM

ROMs are non-volatile. They retain their data even when power is removed from the system and are therefore useful for programs which need to operate as soon as a system is switched on. However, data cannot be changed in them since they are read-only devices. Generally, they have a slightly slower access time than RAM chips.

**Q15** The binary number found in any memory address in a computer system can be classified in one of three ways. What are they? (3 min)

**A15** The binary number found in any memory address may be either

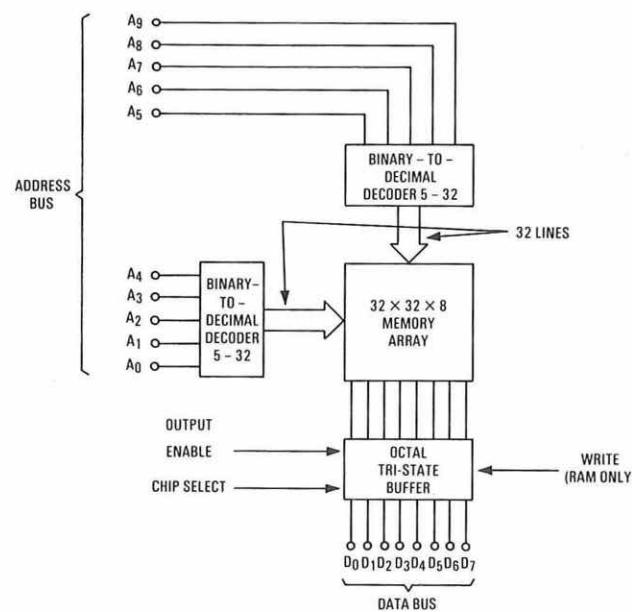
- an instruction to the central processing unit
- a byte of data which is to be used by the program, or
- 'garbage'; that is, information has not been placed in that particular memory address and it, therefore, contains random data that was present just after the computer was switched on.

**Q16** Some devices in computer systems are referred to as having 'tri-state' outputs. Briefly explain what this means. (4 min)

**A16** A tri-state device is one which can have one of three possible states on its output at any moment. These states are logic 1, logic 0, or an open circuit (or very high impedance). The last state is used whenever an output is connected to a common data bus line. If the system does not require an output from a particular chip, it can set the output of the chip in an open-circuit condition so that other devices can then use the common data highway.

**Q17** Draw a block diagram to show the internal structure of a typical memory device, making sure that it is clear where the address and data lines are connected. (5 min)

**A17** The internal structure of a typical memory device is shown in the sketch.



**Q18** Describe the function of a unidirectional buffer and a bidirectional buffer and briefly explain where each one can be found in a microprocessor system. (4 min)

**A18** A unidirectional buffer is a device that is used to improve the current drive capability of an output pin. Since most output pins of microprocessor chips have only limited current output, unidirectional buffers are used to increase this capability and therefore allow them to drive a large number of other devices; that is, a buffer increases the fan-out of any particular output. Unidirectional buffers are generally found in the address bus lines.

A bidirectional buffer consists of two unidirectional buffers connected 'back to back'. It has two data input/output lines and a direction control input. Although it can be used for transmission of data in either direction, only one direction can be used at any moment. They are generally connected in the data bus.

Both types of buffer generally have a control input which allows the output to be placed in an open-circuit (tri-state) condition.

**Q19** Switches provide a very common type of data input to microprocessor-based systems. Briefly describe the major problem associated with accepting data from switches and indicate how this can be overcome. (4 min)

**A19** All switches exhibit 'switch bounce', a condition associated with the closing and opening of mechanical contacts, which rarely happens cleanly. The switch contacts tend to bounce open and closed very rapidly at the time of making or breaking. This can lead to the computer believing that the switch has been turned on and off very quickly and hence leads to false data inputs.

The simplest method of overcoming the problem is to use a software debounce program. This consists of a short time delay, typically 10ms, which can be used so that any bounce of the contacts will have settled before the data is read from the switch. Switch bounce is associated not only with toggle switches but also with keyboard contacts and other types of mechanical input. Alternative methods which require extra hardware, such as latches or resistor capacitor networks, can also be used to overcome the problem, although this would probably be a more expensive solution than a simple delay in the computer program.